

APPLICATION NO.
10/691,111

SUPPLEMENTAL INFORMATION DISCLOSURE
CITATION IN AN APPLICATION

November 19, 2004

(Use several sheets if necessary)

FIRST NAMED INVENTOR
Richard C. Foss

FILING DATE
October 22, 2003

EXAMINER
Hien N. Nguyen

CONFIRMATION NO. 5335	GROUP 2824
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U.S. PATENT DOCUMENTS

[illegible]

EXAMINER

H. NGUYEN

DATE CONSIDERED

2/1/05

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OTHER DOCUMENTS (Including Author, Title, Date, Pertinent Pages, Etc.)

HN	AS	Sugibayashi, T., et al., "A 30ns 256Mb DRAM with Multi-Divided Array Structure," <i>IEEE International Solid-State Circuits Conference</i> , Session 3 (1993).
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HN	AU	Horiguchi, M., et al., "A Flexible Redundancy Technique for High-Density DRAM's," <i>IEEE Journal of Solid-State Circuits</i> , V. 26, No. 1 (1991).
HN	AV	Kimura, K., et al., "A Block-Oriented RAM with Half-Sized DRAM Cell and Quasi-Folded Data-Line Architecture," <i>IEEE Journal of Solid-State Circuits</i> , V. 26, No. 11 (1993).
HN	AW	Kimura, K., et al., "A Block-Oriented RAM with Half-Sized DRAM Cell and Quasi-Folded Data-Line Architecture," <i>IEEE International Solid-State Circuits Conference</i> , Session 6 (1991).
HN	AX	Dosaka, K., et al., "A 100MHz 4Mb Cache DRAM with Fast Copy-Back Scheme," <i>IEEE International Solid-State Circuits Conference</i> , Session 9 (1992).
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EXAMINER H. NGUYEN	DATE CONSIDERED 2/11/05
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